BRIEF SKETCH OF CONTRIBUTIONS

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For the past 50 years, Carver Mead has dedicated his research, teaching, and public presentation to the physics and technology of electron devices. This effort has been divided among basic physics, practical devices, and seeing the solid state as a medium for the realization of novel and enormously concurrent computing structures. Listed below are a number of important contributions that were made over that period.

1960 Proposed and demonstrated the first three-terminal solid-state device operating with electron tunneling and hot-electron transport as its operating principles (1).

1961 Initiated a systematic investigation of the energy-momentum relation of electrons in the energy gap of insulators (2, 3, 4) and semiconductors (5, 6, 7). These studies involved exquisite control of nanometer-scale device dimensions, albeit in only one dimension.

1962 First demonstration that hot electrons in Gold retained their energy for distances in the nanometer range (8).

1963 With W. Spitzer (9, 10, 11), established the systematic role of interface states in determining the energy at interfaces of III-V compounds, independent of the detailed nature of the interface. This work anticipated the role of interfaces in band-gap engineering, which is centrally important in modern heterojunction devices.

1963-1976 With W. Spitzer and many other collaborators and students, undertook a systematic study of the physics and commercial importance of Schottky barriers on a wide range of semiconductors. The understanding gained from these studies ramified in several directions over the following years. Much of the nano-scale work accomplished during the period is directly dependent on knowledge of barrier behavior and tunneling.

1965 Built the first working Schottky-barrier-gate field-effect transistor (12). This device (MESFET) has come to be the standard high-frequency transistor used in satellites, cell phones, and other microwave communications systems. Using modern band-gap-engineered materials, the device is now known as the HEMT.

1969 Gave the first systematic treatment of ohmic contacts to semiconductor devices. These structures were the first true nanometer-scale devices, and are still the most numerous. Showed that they were tunneling junctions and were critically dependent on the doping density of the semiconductor, but not on the metal used (13, 14).

1969 With S. Kurtin and T.C. McGill, demonstrated several manifestations of a fundamental transition in the nature of solids depending on the relative contribution of covalent and ionic bonding. This paper was highly controversial at the time, and was only published after careful review by, and discussions with John Bardeen (15).

1970 With S.T. Hsu and R. Whittier, reported the first single-electron transistors. These were accidental three-dimensional nanometer-scale devices that resulted in field returns of commercial transistors (16).

1970 Taught first VLSI course at Caltech. First Multi-Project Chip. This course and the multi-project shared-wafer methodology that went with it became the model for an entire generation of courses that contributed greatly to innovation around the world (17).

1970 With M. Delbruck, initiated a program to apply the physical principles learned from electron transport through insulating films to ion transport through membranes of biological interest. At the time the common belief was that the exponential current-voltage characteristics of these systems was due to the individual properties of certain nanometer-scale molecules embedded in the membrane. With a number of collaborators (18, 19, 20) established that the characteristics were due to the population statistics of the molecules, and that the individual molecules had an ohmic current-voltage curve. This result is now taken for granted in the biophysics literature, but was quite controversial at the time.

1971 With B. Hoeneisen, showed that Silicon Carbide Schottky-barrier diodes with nanometer-scale depletion layers were vastly more effective high-power rectifiers than conventional Silicon devices (21). This prediction was based on a deep understanding of the tunneling process and measurements of barrier properties on this remarkable material. The potential of these devices was not realized until twenty years later when single-crystal SiC wafers became available. Today these devices are the workhorses of high-power electronics.

1971 With S. Colley, built and demonstrated the first simple Silicon Compiler. Produced both simulation and layout from higher-level functional description (in this case, finite-state machine code). Silicon Compilation was to be the centerpiece of the next 15 years' work, motivating many of the more detailed contributions. By 1991, every major chip-design effort in the world used some variant of this key technology.

1972 As the culmination of many years of work in solid-state device physics, published (with B. Hoeneisen) the first prediction of the nanometer-scale lower limit to the size of transistors (22). These limits were based on fundamental physical laws, and were much smaller than generally expected. These predictions, along with the general notions of scalability that went with them, were instrumental in setting the industry on its path toward nanometer-scale technology. The limits established at that time have held up to the present day, in the face of many years of experimental and theoretical work done at laboratories throughout the world (23). Because these results formed the scientific basis underlying Moore's Law, they have had enormous economic impact worldwide.

1972 With A. Mohsen, T. McGill, and Y. Daimon, gave the first quantitative treatment of charge transfer efficiency in overlapping-gate CCD structures (24, 25, 26). A new clocking methodology was invented, which allowed a considerable increase in both charge capacity and transfer efficiency (27). This work formed the basis for the high transfer-efficiency CCD devices now used for imaging applications.

1976 Described two unique concurrent computing structures: a serial compare-under-mask chip (class project from the first VLSI course, actually finished in 1971), and (with E. Cheng and R. Lyon), a serial pipelined multiplier. Articulated the concept that pipelined structures passing data to nearest neighbors formed an optimal VLSI structure. This principle paved the way for much more general work on systolic algorithms.

1977 Distilled many of these thoughts into an article, written jointly with Ivan Sutherland, in *Scientific American* (28). This popular account was the first that received any attention from the Computer Science community.

1978 With M. Rem, proposed the foundations of a Complexity Theory for VLSI, in which time, area, and energy were the dimensions of a cost vector (29, 30). This work has led to a fundamental expansion in the notion of computational complexity.

1979 Gave the first public discussion of the role of silicon foundries in promoting technological innovation (31). The first Caltech conference on VLSI, at which that talk was given, was also the occasion of the first description of Dave Johannsen's graduate research on silicon compilation, and was the first time the term had been coined. The coincidence of silicon compilation (now called Synthesis) and Silicon Foundries (32) led to an entire new business model for the semiconductor industry, now called Fabless Semiconductor. This segment is currently responsible for over half the economic value of the entire semiconductor industry.

1979 Articulated the impact that the VLSI technology would have on Computer Science education, a set of predictions that have now appeared in the standard curricula (33).

1979 The book, *Introduction to VLSI Systems*, written with Lynn Conway as co-author, appeared (34). This book captured many of the insights of the previous 10 years' work in a form that could be taught to students with a wide variety of backgrounds.

1982 With M. Chen, presented the first formal semantics for general VLSI systems (35). This work led to a completely general hierarchical approach to system specification and simulation (36, 37, 38, 39).

1983 With T. Lin, extended the hierarchical semantics work to include a physically based treatment of time delay (40, 41, 42, 43).

2007 With J. Wawrzynek, described a very general concurrent computational approach to problems requiring the solution of finite-difference equations in *time*. Used the approach to produce high-quality musical instruments in real time. The structure used for this application was a programmable interconnect technology that became the basis for a large class of commercial Field-Programmable Gate Arrays (44, 45, 46).

1984 With M. A. Mahowald, described the first analog silicon retina (47). The approach to silicon models of certain neural computations expressed in this chip, and its successors, foreshadowed a totally new class of physically based computations inspired by the neural paradigm. More recent results demonstrated that a wide range of visual and auditory computations of enormous complexity can be carried out in minimal area and with minute energy dissipation compared with digital implementations.

1984 The book *Analog VLSI and Neural Systems* was published (48). This book condensed the insights gained during the previous eight years of work into a single volume, accessible to students with a wide range of backgrounds. Several recent reviews have spelled out in some detail the compelling advantages of realizing adaptive systems directly in analog VLSI. Reduction of system power dissipation by a factor of 10,000, and of silicon area by a factor of 100 are being demonstrated.

1985-1998 Experience gained in using photo-response of semiconductor structures for barrier-energy and band-gap studies led to system-level structures that sensed and processed images in various ways. With numerous collaborators, a large variety of imaging structures were developed. One branch of this effort resulted in CMOS imagers, now the most prevalent of all image sensors. A particular subset of these, the X3 sensors, have produced some of the finest images ever captured by any photographic technology.

1972-2000 Throughout the entire period, worked to bring about a general awareness of Computation as a physical process, rather than purely a mathematical one. Strongly advocated the importance of unifying technology and architecture into a single discipline, and emphasized the importance of this unity for the future of the field at large.

2000 The book *Collective Electrodynamics: Quantum Foundations of Electromagnetism,* published by MIT Press, unifies electromagnetic phenomena with the quantum nature of matter (49).

2007-Present Recent work on Collective Electrodynamics is evolving an entire introductory level physics course based on macroscopic quantum systems. This approach allows students to develop a deep intuition for fundamental physical processes by way of simple laboratory experiments.

REFERENCES

1. Mead, C., **The Tunnel Emission Amplifier**, *Proceedings of the IRE*, vol. 48, pp. 359–361, 1960.
2. Mead, C., **Tunneling Physics**, *Colloquium of Solid State Devices*, Office for Industrial Associates, pp. 13–21, 1961.
3. Mead, C., **Electron Transport Mechanisms in Thin Insulating Films**, *The Physical Review*, vol. 128, pp. 2088–2093, 1962.

4. McColl, M. and Mead, C., **Electron Current Through Thin Mica Films**, *Transactions of the Metallurgical Society of AIME*, vol. 233, pp. 502–511, 1964.
5. Lewicki, G. and Mead, C., **Experimental Determination of E-*k* Relationship in Electron Tunneling**, *Physical Review Letters*, vol. 16, pp. 939–941, 1966.
6. Snow, E.H., Deal, B.E. and Mead, C., **Barrier Lowering and Field Penetration at Metal-Dielectric Interfaces**, *Applied Physics Letters*, vol. 9, pp. 53–55, 1966.
7. Parker, G.H. and Mead, C., **Energy-Momentum Relationship in InAs**, *Physical Review Letters*, vol. 21, pp. 605–607, 1968.
8. Mead, C., **Transport of Hot Electrons in Thin Gold Films**, *Physical Review Letters*, vol. 8., pp. 56–57, 1962.
9. Mead, C.A. and Spitzer, W.G., **Fermi Level Position at Semiconductor Surfaces**, *Physical Review Letters*, vol. 10, pp. 471–472, 1963.
10. Spitzer, W.G. and Mead, C.A., **Barrier Height Studies on Metal-Semiconductor Systems**, *Journal of Applied Physics*, vol. 34, pp. 3061–3069, 1963.
11. Mead C.A. and Spitzer, W.G., **Fermi Level Position at Metal-Semiconductor Interfaces**, *The Physical Review*, vol. 134, pp. A713–A716, 1964.
12. Mead, C., **Schottky Barrier Gate Field Effect Transistor**, *Proceedings of IEEE*, vol. 54, pp. 307–308, 1966.
13. Mead, C., **Physics of Interfaces**, Schwartz, B., *Ohmic Contacts to Semiconductors*, New York, NY: Electrochemical Society, 1969, pp. 3–16.
14. Mead, C., **Some Properties of Exponentially Damped Wave Functions**, Burstein, E. and Lundqvist, S., *Tunneling Phenomena in Solids; Lectures*, New York, NY: Plenum Press, 1969, pp. 127–134.
15. Kurtin, S., McGill, T.C. and Mead C., **Fundamental Transition in the Electronic Nature of Solids**, *Physical Review Letters*, vol. 22, pp. 1433–1436, 1969.
16. Hsu, S.T., Whittier, R.J. and Mead, C., **Physical Model for Burst Noise in Semiconductor Devices**, *Solid-State Electronics*, vol. 13, pp. 1055–1071, 1970.
17. Mead, C., **Computers That Put the Power Where It Belongs,** *Engineering and Science,* vol. XXXVI, No. 4, pp. 4–9, February, 1972.
18. Kauffman, J.W. and Mead, C., **Electrical Characteristics of Sphingomyelin Bilayer Membranes**, *Biophysical Journal*, vol. 10, pp. 1084–1089, 1970.
19. Hall, J.E., Mead, C. and Szabo, G., **A Barrier Model for Current Flow in Lipid Bilayers Membranes**, *Journal of Membrane Biology*, vol. 11, pp. 75–97, 1973.
20. Eisenberg, M., Hall, J.E. and Mead, C., **The Nature of the Voltage-Dependent Conductance Induced by Alamethicin in Black Lipid Membranes**, *Journal of Membrane Biology*, vol. 14, pp. 143–176, 1976.
21. Hoeneisen, B. and Mead, C., **Power Schottky Diode Design and Comparison With the Junction Diode**, *Solid-State Electronics*, vol. 14, pp. 1225–1236, 1971.
22. Hoeneisen, B. and Mead, C., **Fundamental Limitations in Microelectronic–I, MOS Technology**, *Solid-State Electronics*, vol. 15, pp. 819–829, 1972.

23. Mead, C., **Scaling of MOS Technology to Submicrometer Feature Sizes**, *Journal of VLSI Signal Processing*, vol. 8, pp. 9–25, 1994.

24. Mohsen, A.M., McGill, T.C. and Mead, C., **Charge Transfer in Charge-Coupled Devices**, Winner, L., *Digest of Technical Papers, 1972 IEEE International Solid-State Circuits Conference*, New York, NY: Lewis Winner, 1972, pp. 248–249.
25. Mohsen, A.M., McGill, T.C., Daimon, Y. and Mead, C., **The Influence of Interface States on Incomplete Charge Transfer in Overlapping Gate Charge-Coupled Devices**, *IEEE Journal of Solid-State Circuits*, SC-8, pp. 125–138, 1973.
26. Mohsen, A.M., McGill, T.C. and Mead, C., **Charge Transfer in Overlapping Gate Charge-Coupled Devices**, *IEEE Journal of Solid-State Circuits*, SC-8, pp. 191–206, 1973.
27. Mohsen, A.M., McGill, T.C., Anthony, M. and Mead, C., **Push Clocks: A New Approach to Charge-Coupled Devices Clocking**, *Applied Physics Letters*, vol. 22, pp. 172–175, 1973.
28. Sutherland, I.E. and Mead, C., **Microelectronics and Computer Science**, *Scientific American*, vol. 237, pp. 210–228, 1977.
29. Rem, M. and Mead, C., **Cost and Performance of VLSI Computing Structures**, Elmasry, M.I., *Digital MOS Integrated Circuits*, New York, NY: IEEE Press, 1981, pp. 196–203, (Reprinted from: *IEEE Journal of Solid State Circuits*, SC-14, pp. 455–462, 1979; Also published as *Caltech Computer Science Technical Report, 1584:TR:78.*).
30. Rem, M. and Mead, C., **Minimum Propagation Delays in VLSI**, Seitz, C., *Proceedings of Second Caltech Conference on Very Large Scale Integration*, Pasadena, CA: California Institute of Technology, 1981, pp. 433–439 (Also published as *Caltech Computer Science Technical Report, 4601:TR:81.*).
31. Mead, C., **VLSI and Technological Innovation**, Seitz, C., *Proceedings of Caltech Conference on Very Large Scale Integration*, Pasadena, CA: California Institute of Technology, pp. 15–27, 1979.
32. Mead, C.A. and Lewicki, G., **Silicon Compilers and Foundries Will Usher in User-Designed VLSI**, *Electronics*, vol. 55, pp. 107–111, 1982.
33. Mead, C., **The Impact of VLSI on Computer Science Education**, *IEEE Transactions on Education*, vol. 22, pp. 43, 1979.
34. Mead, C. and Conway, L., **Introduction to VLSI Systems**, Reading, MA: Addison-Wesley, 1980.
35. Chen, M. and Mead, C., **Formal Specification of Concurrent Systems**, *Caltech Computer Science Technical Report, 5042:TR:82*, California Institute of Technology, Pasadena, 1982 (Contains two papers: *VLSI Signal Processing and Formal Semantics, Concurrent Algorithms as Space-Time Recursion Equations*.)
36. Chen, M. and Mead, C., **VLSI Circuits as Communicating Processes: A Universal Simulator**, *International Symposium on VLSI Technology, Systems and Applications*, March 30–April 1, 1983, Taipei, Taiwan, Hsinchu, Taiwan: ERSO, ITRI, pp. 302–306, 1983.
37. Chen, M. and Mead, C., **A Hierarchical Simulator Based on Formal Semantics**, Bryant, R., *Third Caltech Conference on Very Large Scale Integration, 1983*, Rockville, MD: Computer Science Press, 1983, pp. 207–223 (Also published as *Caltech Computer Science Technical Report, 5068:TM:83.*).

38. Chen, M. and Mead, C., **A Methodology for Hierarchical Simulation and Verification of VLSI Systems**, Giloi, W.K. and Shriver, B.D. (eds), *Methodologies for Computer System Design: Proceedings for the IFIP WG 10.1 Working Conference, Lille, France, 1983*, North Holland, Amsterdam: Elsevier Science, 1985, pp. 165–181.
39. Chen, M. and Mead, C., **The Semantics of a Functional Language for VLSI Systems**, Giloi, W.K. and Shriver, B.D. (eds), *Methodologies for Computer System Design: Proceedings for the IFIP WG 10.1 Working Conference, Lille, France, 1983*, North Holland, Amsterdam: Elsevier Science, 1985, pp. 1–18.
40. Lin, T.M. and Mead C., **Signal Delay in General RC Networks with Application to Timing Simulation of Digital Integrated Circuits**, *Caltech Computer Science Technical Report, 5089:TR:83*, California Institute of Technology, Pasadena, 1983.
41. Lin, T.M. and Mead C., **Signal Delay in General RC Networks**, *IEEE Transactions on Computer-Aided Design*, CAD-3, pp. 331–349, 1984.
42. Lin, T.M. and Mead, C., **Signal Delay in General RC Networks with Application to Timing Simulation of Digital Integrated Circuits**, Penfield, P., *Proceedings, Conference on Advanced Research in VLSI*, Dedham, MA: Artech House, 1984, pp. 93–99.
43. Lin, T.M. and Mead, C., **A Hierarchical Timing Simulation Model**, *IEEE Transactions on Computer-Aided Design*, CAD-5, pp. 188–197, 1986.
44. Wawrzynek, J. and Mead, C., **A VLSI Approach to Sound Synthesis**, Denyer, P.B., *VLSI Signal Processing: A Bit-Serial Approach*, Reading, MA: Addison-Wesley, 1985 (Also published as a *Caltech Computer Science Technical Report, 5158:TR:84*.).
45. Wawrzynek, J., Mead, C., Lin, T.M., Liu, H. and Dyer, L., **A VLSI Approach to Sound Synthesis**, Buxton, W., *Proceedings of the International Computer Music Conference, IRCAM*, San Francisco, CA: Computer Music Association, 1985, pp. 53–64.
46. Wawrzynek, J. and Mead, C., **A New Discipline for CMOS Design: an Architecture for Sound Synthesis**, Fuchs, H., *1985 Chapel Hill Conference on Very Large Scale Integration*, Rockville, MD: Computer Science Press, 1985, pp. 87–104.
47. Mahowald, M. and Mead, C., **A Silicon Model of Early Visual Processing**, *Neural Networks*, vol. 1, pp. 91–97, 1988.
48. Mead, C., **Analog VLSI and Neural Systems**, Reading, MA: Addison-Wesley, 1989.
49. Mead, C., **Collective Electrodynamics: Quantum Foundations of Electromagnetism,** Cambridge, MA: The MIT Press, 2000.